XA-9472

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.: 09/855,660 Group Art Unit: 2819

Filed: May 16, 2001 Examiner: D. Chang

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING MEDIUM THEREOF

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AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Prior to continued examination, and in response to the Office Action mailed October 18, 2002, please amend the above-identified patent application as indicated below.

IN THE CLAIMS:

59. (Amended) A design data recording medium according to claim 37,